SmartMesh® IP DN6000 / M600x
2.4 GHz 802.15.4 Mote-on-Chip and Mote Modules

About SmartMesh IP

Dust Networks' new standards-based SmartMesh® IP product line achieves unsurpassed levels of networking resilience and reliability, with advanced network management and comprehensive security. Based on Dust's breakthrough Eterna™ SoC technology, SmartMesh IP enables up to 8x lower power consumption than competing solutions even in harsh, dynamically changing RF environments. Cost effective, IP compatible, and widely applicable, SmartMesh IP serves an extensive range of applications, such as energy management, building automation, renewable energy, and other implementations in smart infrastructure that call for ultra low power. SmartMesh IP has an optional feature that provides for location awareness, which allows you to report the physical location of your mote upon request.

Product Descriptions - DN6000 / M600x

SmartMesh IP networks are populated by motes (the nodes on the network), which are the foundational building blocks required to deploy resilient, reliable, low power, multi-hop wireless mesh networks. Dust motes deliver unprecedented low power consumption with a receive current of less than 5 mA and a transmit current of less than 10 mA at 8dBm (< 6 mA at 0 dBm). With Dust's time-synchronized SmartMesh IP networking, all motes in the network may route and may be battery, energy-harvested, or line powered. SmartMesh IP networks enable multi-year battery life for all motes in the network, including the heaviest routing ones on a CR2032 coin cell.

SmartMesh IP 802.15.4 motes come in two form factors—the DN6000 Mote-on-Chip in an easy-to-integrate 72 pin 10 mm x 10 mm QFN package and the M600*x* series, a 42 mm x 24 mm surface-mount module incorporating the DN6000 Mote-on-Chip. The M6000 module includes a U.FL antenna connector, while the M6001 includes an on-board chip antenna. Both M600*x* will come with modular certifications for FCC, CE, and IC.

The DN6000/M600*x* provides support for direct connection to sensors/actuators (for example, on-board temperature, analog, digital, SPI, I^{2}C, 1-Wire®) as well as an API-driven UART interface for communicating with an external OEM microprocessor, making Dust motes the perfect choice for a large variety of sensor solutions. Coupled with its best-in-class power consumption, the DN6000/M600x is ideal for use in applications that demand reliable performance, ultra-low power operation, and easy expandability.

Key Features

- Based on 6LoWPAN and IEEE 802.15.4e for end-to-end connectivity
- 8x Lower power with Eterna™
  - Radio receive: <5 mA
  - Radio transmit: <6 mA
- Single node type
- Battery powered routers
- Highly accurate time stamping
- Silent RF mode
- Location aware
- Energy harvesting support

Fully Integrated

- RF, micro, flash, and PA integrated in a single SoC
- On-chip PMU with intelligent DC-DC converters and regulators
- Minimum number of external components
- Pre-engineered RF
- Antenna ready
- Multiple peripheral interfaces
- Integrated temperature sensor

Development Tools

- Advanced software design for simple integration
- Evaluation kits available

General

- ROHS-compliant 72-pin QFN 10 mm x 10 mm

Table of Contents

1.0 Features

1.1 SmartMesh IP networking

The DN6000/M600*x* motes ensure reliable connection with the wireless mesh network:

- **Networking joining**—maintains the device security credentials and performs packet exchange with the network manager to join the network
- **Link table tracking**—each mote tracks its own copy of the manager-assigned link table - the time-slotted schedule to be able to transmit to and receive from each neighbor. This enables motes to accept more bandwidth from the network manager.
- **Health reports**—periodically reports to the network manager the network statistics vital to maintaining the network.

1.2 Radio

The DN6000/M600x is the lowest power commercially available 2.4 GHz IEEE 802.15.4e radio by a substantial margin. (Please refer to section 6.2 for current consumption numbers.) In addition to the functionality required to be a 2.4 GHz IEEE 802.15.4e transmitter, the DN6000/M600x's transmitter supports calibrated and temperature-compensated output power optimized to consistently provide power at a limit suitable for worldwide radio certifications. Additionally, the DN6000/M600x leverages its MAC Co-Processor (MCP), which handles precise sequencing of radio-related functions, and other coprocessors like its AES engine to minimize its usage of the CPU, thereby further decreasing power consumption.

1.2.1 External PA/LNA Control

The DN6000/M600x features an on-board Power Amplifier (PA), optimized for +8 dBm conducted RF output power for worldwide license-free operation in the 2.4 to 2.4835-GHz frequency band. For controlling an external PA and/or LNA, the DN6000/M600x's MCP drives signals for external LNA enable (LNA_EN), and external PA enable and switch control (active high RADIO_TX and active low RADIO_TXn).

1.2.2 Radio Inhibit

The RADIO_INHIBIT digital interrupt enables an external controller to temporarily disable the radio software drivers (for example, to take a sensor reading that is susceptible to radio interference). When asserted, the software radio drivers will disallow any radio clear channel assessment, packet transmits, or packet receipts. If a radio event is in progress radio inhibit will take effect after the present operation completes.

1.3 Power Management Unit and Intelligent DC/DC Converters

The DN6000/M600x PMU module controls the power sequencing of the on-chip DC/DC converters and on-chip regulators, clock generation and gating during power up, reset sequencing, and dynamic clock scaling, ensuring proper transitions from power-on on through the Active state and in and out of Doze state. The PMU also manages manual per-module reset and clock gating functions.

1.4 Advanced Software Design for Simple Integration

The DN6000/M600*x* may operate in a variety of software control modes to accommodate different OEM designs:

- **Direct connection to sensors/actuators—**the DN6000/M600x includes a software application layer that may be configured to control the on-board temperature, or sensors/actuators connected via analog input, digital I/O, SPI, I^2C, or 1-Wire. This is ideal for creating small, simple sensing devices, such as peel and stick temperature sensors.
- **API-driven UART interface—**the mote may be controlled via API commands by an external OEM microprocessor. This configuration is often used when adding wireless to an existing product.
- **Hybrid mode—**in this mode, the mote is driven via API and is controlling its own sensors/peripherals. This is often useful when augmenting an existing OEM's device with not only wireless but also additional peripherals, such as the on-board temperature sensor.

1.5 OTAP

The DN6000/M600x supports over-the-air-programming (OTAP). This is very helpful in updating firmware on motes installed in the field for updating features or for fixes.

2.0 Hardware Operating Modes

This section explains the DN6000/M600x hardware operating modes, covering behavior during both start up and operation, as well as the DN6000/M600x's various power modes and duty cycling capabilities.

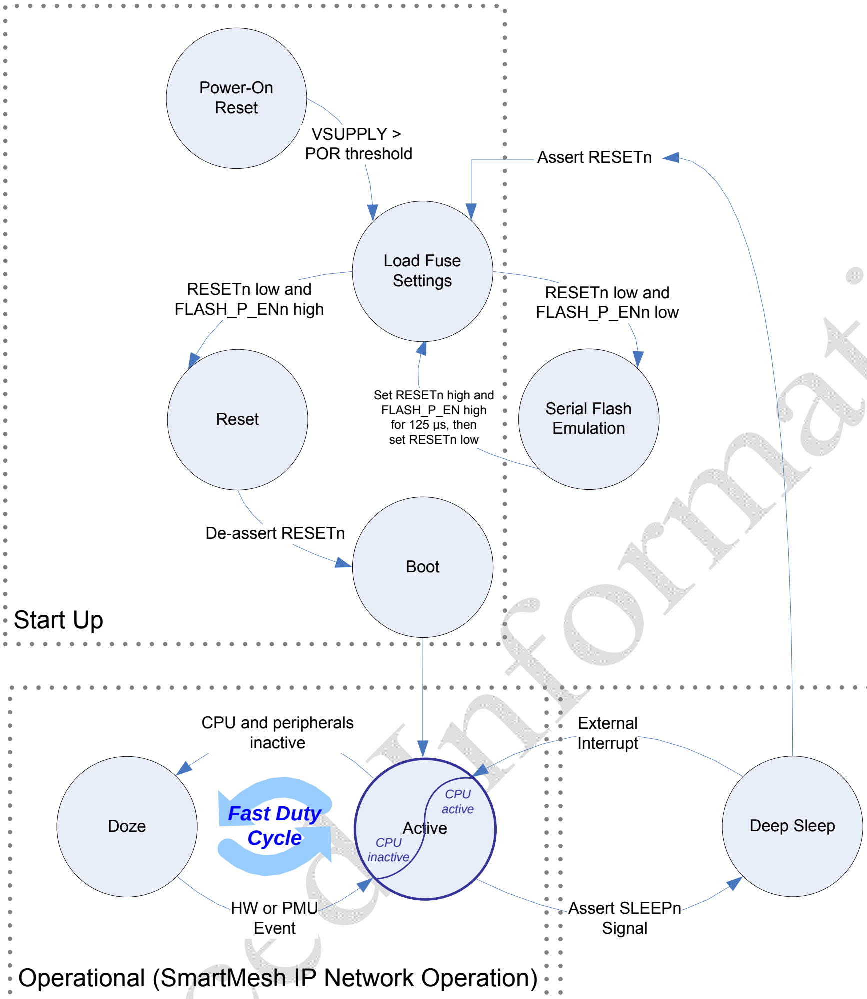


Figure 1 State Diagram – Operating Modes

2.1 Start Up

When power is applied, the DN6000/M600x enters a power-on reset state. Once VSUPPLY reaches the power-on-reset threshold voltage (see section 3.3.1) or RESETn is asserted, the DN6000/M600x transitions to a state in which it loads its fuse settings (see section 3.19), including setting I/O direction. In this state, the DN6000/M600x checks the state of the FLASH_P_ENn and RESETn and enters the serial flash emulation mode, if both signals are asserted. If the FLASH_P_ENn pin is not asserted, the DN6000/M600x enters a low power Reset state by disabling the internal relaxation oscillator until RESETn is released. Once RESETn is de-asserted, the DN6000/M600x goes through a boot sequence, and then enters the Active state.

2.2 Serial Flash Emulation

When both RESETn and FLASH_P_ENn are asserted, the DN6000/M600x disables normal operation and enters a mode to emulate the operation of a serial flash. In this mode, its flash can be programmed with software updates. For details, see section 3.17.

2.3 Operational

Once the DN6000/M600*x* has completed startup, it transitions to the Operational group of states (Active with its CPU states and Doze). There, the mote cycles between the various states, automatically selecting the lowest power state possible while fulfilling the demands of SmartMesh IP network operation.

2.3.1 Active State

In Active state, the internal relaxation oscillator is running and peripherals are enabled as needed. The ARM® Cortex™-M3 may cycle as needed between CPU-active and CPU-sleep (referred to in the ARM Cortex-M3 literature as “Sleep Now” or “Sleep on Exit” modes). The DN6000/M600x’s system of internal co-processors minimizes the time the CPU must remain awake for peripheral operations by controlling many peripheral operations with very low power.

2.3.2 Doze State

The Doze state typically consumes several orders of magnitude less current than the Active state (see Table 9) and is entered when all of the peripherals and the CPU are inactive. In Doze state, the device’s state is retained. In the Doze state the device will sense activity on GPIOs configured as interrupts, the UART ports, and the SPI slave port. Additionally, the 32.768-kHz oscillator and timers are active, including the watchdog timeout. As the DN6000/M600x has an internal relaxation oscillator that can start quickly, the DN6000/M600x can typically transition from Doze to Active within 5 µs.

2.4 Fast Duty Cycling

The DN6000/M600x’s ability to quickly transition between Doze and Active states, coupled with the fact that these transitions are energy efficient (see Table 16) enables Fast Duty Cycling to drastically reduce power consumption on a very granular timescale. For example, the system can automatically go from Doze to Active without CPU interruption, and then detect the RF channel energy and wake the CPU if a packet is detected, otherwise returning to Doze.

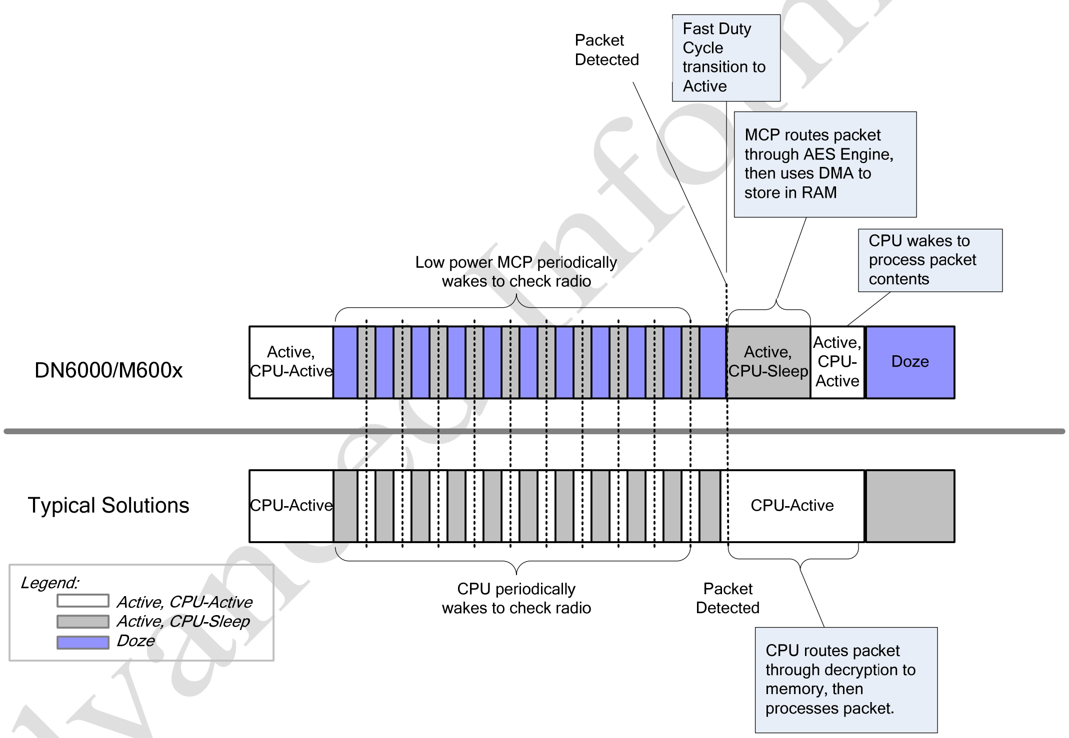


Figure 2 Fast Duty Cycling

2.5 Deep Sleep State

The DN6000/M600x also features a Deep Sleep state (with lower power than Doze), in which the DN6000/M600x has full RAM retention and all other features of Doze state, but the 32.768-kHz oscillator is off. The DN6000/M600x will enter the Deep Sleep state when the SLEEPn external interrupt is asserted. The DN6000/M600x may be awakened from Deep Sleep via an external hardware interrupt or by asserting the RESETn hardware reset.

3.0 Pinout

3.1 DN6000 Mote-on-Chip

Figure 3 shows default pinout for the DN6000 Mote-on-Chip. Pins are grouped by function. In some cases, a pin may have multiple possible functions; the behavior is determined by the software application layer.

Note: All unused input pins must be driven to an inactive state to avoid excess leakage and undesired operation. Leakage due to floating inputs can be substantially greater than the average power consumption.

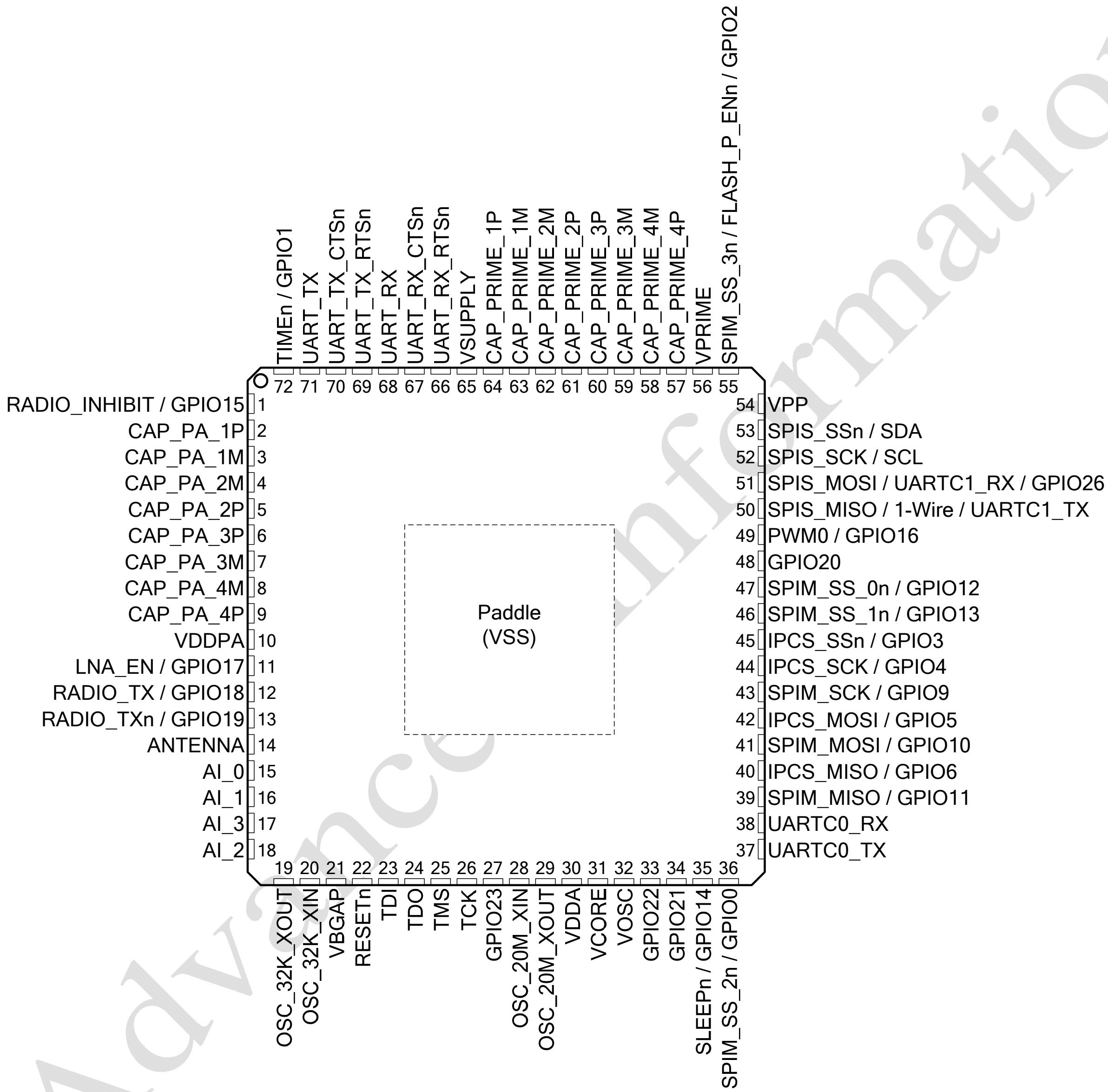


Figure 3 DN6000 Mote-on-Chip Pinout – Top View

Table 1 DN6000 Mote-on-Chip Pinout Assignments

No	Power Supply	Type	I / O	Description
P	GND	Power	-	Ground connection P = QFN Paddle
2	CAP_PA_1P	Power	-	PA DC/DC converter capacitor 1 plus terminal
3	CAP_PA_1M	Power	-	PA DC/DC converter capacitor 1 minus terminal
4	CAP_PA_2M	Power	-	PA DC/DC converter capacitor 2 minus terminal
5	CAP_PA_2P	Power	-	PA DC/DC converter capacitor 2 plus terminal
6	CAP_PA_3P	Power	-	PA DC/DC converter capacitor 3 plus terminal
7	CAP_PA_3M	Power	-	PA DC/DC converter capacitor 3 minus terminal
8	CAP_PA_4M	Power	-	PA DC/DC converter capacitor 4 minus terminal
9	CAP_PA_4P	Power	-	PA DC/DC converter capacitor 4 plus terminal
10	VDDPA	Power	-	Internal power amplifier power supply
21	VBGAP	Analog	O	Do not connect
30	VDDA	Power	-	Regulated analog core supply
31	VCORE	Power	-	Regulated core supply
32	VOSC	Power	-	Regulated oscillator supply
54	VPP	-	-	Test – do not connect
56	VPRIME	Power	-	Internal primary core power supply
57	CAP_PRIME_4P	Power	-	Primary DC/DC converter capacitor 4 plus terminal
58	CAP_PRIME_4M	Power	-	Primary DC/DC converter capacitor 4 minus terminal
59	CAP_PRIME_3M	Power	-	Primary DC/DC converter capacitor 3 minus terminal
60	CAP_PRIME_3P	Power	-	Primary DC/DC converter capacitor 3 plus terminal
61	CAP_PRIME_2P	Power	-	Primary DC/DC converter capacitor 2 plus terminal
62	CAP_PRIME_2M	Power	-	Primary DC/DC converter capacitor 2 minus terminal
63	CAP_PRIME_1M	Power	-	Primary DC/DC converter capacitor 1 minus terminal
64	CAP_PRIME_1P	Power	-	Primary DC/DC converter capacitor 1 plus terminal
65	VSUPPLY	Power	-	Power supply input to the DN6000
No	**Radio**	**Type**	**I / O**	**Description**
1	RADIO_INHIBIT GPIO15	1	I I/O	Radio Inhibit General purpose digital I/O
11	LNA_EN GPIO17	1	O I/O	External LNA enable General purpose digital I/O
12	RADIO_TX GPIO18	1	O I/O	Radio TX active (external PA enable/switch control) General purpose digital I/O
13	RADIO_TXn GPIO19	1	O I/O	Radio TX active (external PA enable/switch control), active low General purpose digital I/O
14	ANTENNA	-	-	Single ended antenna port
No	**Analog**	**Type**	**I / O**	**Description**
15	AI_0	Analog	I	Analog input 0
16	AI_1	Analog	I	Analog input 1
17	AI_3	Analog	I	Analog input 3
18	AI_2	Analog	I	Analog input 2

No	Crystals	Type	I/O	Description
19	OSC_32K_XOUT	Crystal	I	32 kHz crystal xout
20	OSC_32K_XIN	Crystal	I	32 kHz crystal xin
28	OSC_20M_XIN	Crystal	I	20 MHz crystal xin
29	OSC_20M_XOUT	Crystal	I	20 MHz crystal xout

No	Reset	Type	I/O	Description
22	RESETn	1	I	Reset, Input, active low
No	**JTAG**	**Type**	**I/O**	**Description**
23	TDI	1	I	JTAG test data in
24	TDO	1	O	JTAG test data out
25	TMS	1	I	JTAG test mode select
26	TCK	1	I	JTAG test clock
No	**GPIOs**	**Type**	**I/O**	**Description**
27	GPIO23	1	I/O	General purpose digital I/O
33	GPIO22	1	I/O	General purpose digital I/O
34	GPIO21	1	I/O	General purpose digital I/O
48	GPIO20	1	I/O	General purpose digital I/O
Note: See also pins 1, 11, 12, 13, 35, 36, 39, 40, 41, 42, 43, 44, 45, 46, 47, 49, 51, 55 and 72 for additional GPIO ports.				
No	**Special Purpose Digital**	**Type**	**I/O**	**Description**
35	SLEEPn GPIO14	1 1	I I/O	Deep Sleep, active low General purpose digital I/O
49	PWM0 GPIO16	2	O I/O	Pulse width modulator 0 General purpose digital I/O
72	TIMEn GPIO1	1	I I/O	Time capture request, active low General purpose digital I/O
No	**CLI**	**Type**	**I/O**	**Description**
37	UARTC0_TX	2	O	CLI UART 0 transmit
38	UARTC0_RX	1	I	CLI UART 0 receive
No	**SPI Master**	**Type**	**I/O**	**Description**
36	SPIM_SS_2n GPIO0	1	O I/O	SPI master slave select 2, active low General purpose digital I/O
39	SPIM_MISO GPIO11	1	I I/O	SPI master (MISO) master in slave out port General purpose digital I/O
41	SPIM_MOSI GPIO10	2	O I/O	SPI master (MOSI) master out slave in port General purpose digital I/O
43	SPIM_SCK GPIO9	2	O I/O	SPI master (SCK) serial clock port General purpose digital I/O
46	SPIM_SS_1n GPIO13	1	O I/O	SPI master slave select 1, active low General purpose digital I/O
47	SPIM_SS_0n GPIO12	1	O I/O	SPI master slave select 0, active low General purpose digital I/O
55	SPIM_SS_3n FLASH_P_ENn GPIO2	1	O I I/O	SPI master slave select 3, active low. Flash program enable, active low Note that this functionality is available only when RESETn is asserted General purpose digital I/O

No	SPI Slave/FLASH Programming	Type	I/O	Description
40	IPCS_MISO GPIO6	2	O I/O	SPI flash emulation (MISO) master in slave out port General purpose digital I/O
42	IPCS_MOSI GPIO5	1	I I/O	SPI flash emulation (MOSI) master out slave in port General purpose digital I/O
44	IPCS_SCK GPIO4	1	I I/O	SPI flash emulation (SCK) serial clock port General purpose digital I/O
45	IPCS_SSn GPIO3	1	I I/O	SPI flash emulation slave select, active low General purpose digital I/O
Note: See also pin 55 under SPI master for FLASH_P_ENn functionality.				

No	I^2C/1-Wire / SPI Slave 2	Type	I/O	Description
50	SPIS_MISO 1-WIRE UARTC1_TX	2	O O O	SPI slave (MISO) master in slave out port 1-Wire UART 1 transmit
51	SPIS_MOSI UARTC1_RX GPIO26	1	I I I/O	SPI slave (MOSI) master out slave in port UART 1 receive General purpose digital I/O
52	SPIS_SCK SCL	2	I I/O	SPI slave (SCK) serial clock port I^2C serial clock
53	SPIS_SSn SDA	2	I I/O	SPI slave select, active low I^2C serial data

No	UART	Type	I/O	Description
66	UART_RX_RTSn	1	I	UART receive (RTS) request to send, active low
67	UART_RX_CTSn	1	O	UART receive (CTS) clear to send, active low
68	UART_RX	1	I	UART receive
69	UART_TX_RTSn	1	O	UART transmit (RTS) request to send, active low
70	UART_TX_CTSn	1	I	UART transmit (CTS) clear to send, active low
71	UART_TX	2	O	UART transmit
Note: See also pins 50, 51 for an additional UART port.				

3.2 M600*x* Mote Modules

The M6000 and M6001 mote modules are shown in Figure 4 and Figure 5. Pins are described in Table 2, where they are grouped by function. In some cases, a pin may have multiple possible functions.

Note: All unused input pins must be driven to an inactive state to avoid excess leakage and undesired operation. Leakage due to floating inputs can be substantially greater than the average power consumption.

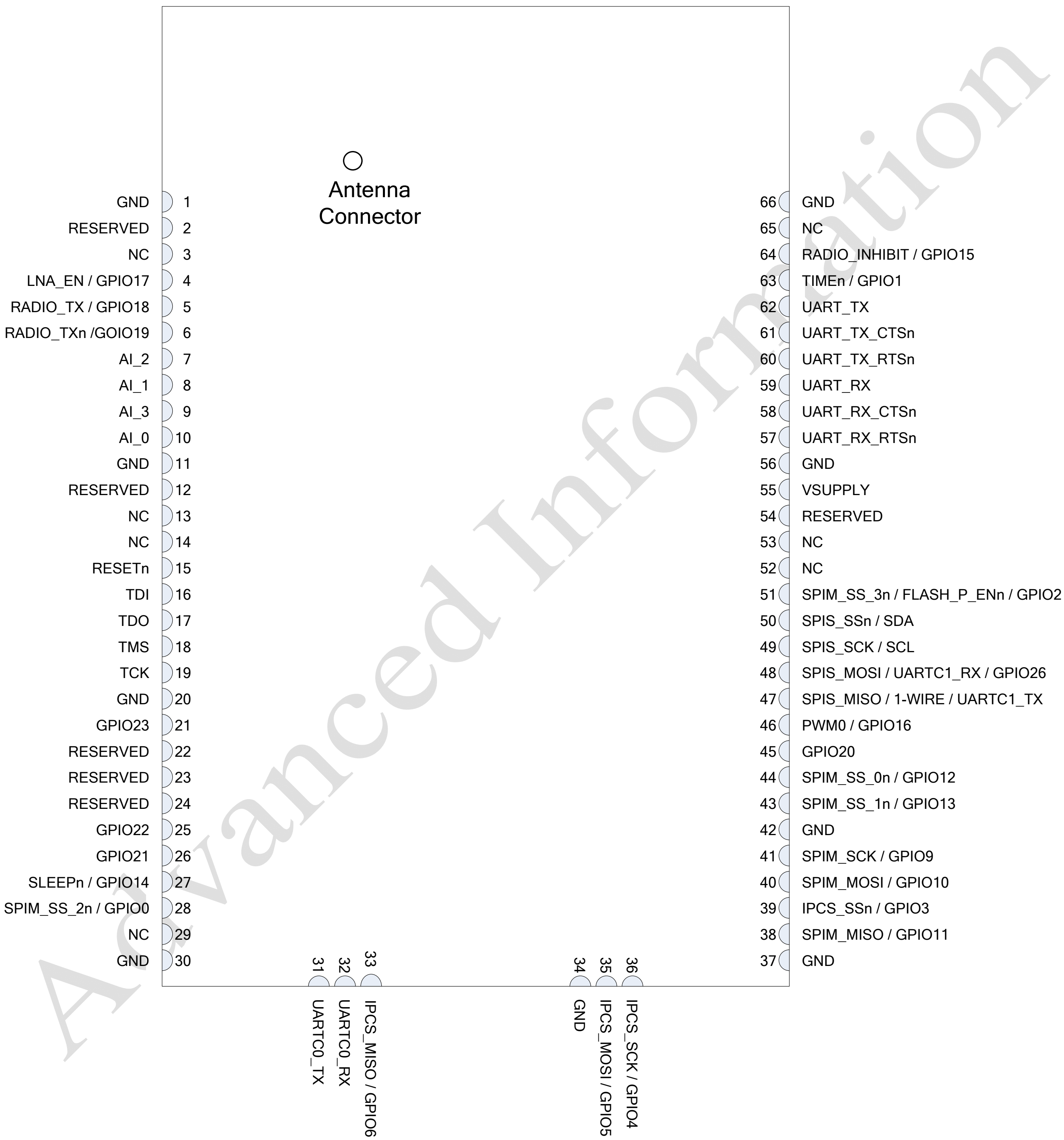


Figure 4 M6000 – Mote Module with U.FL Antenna Connector

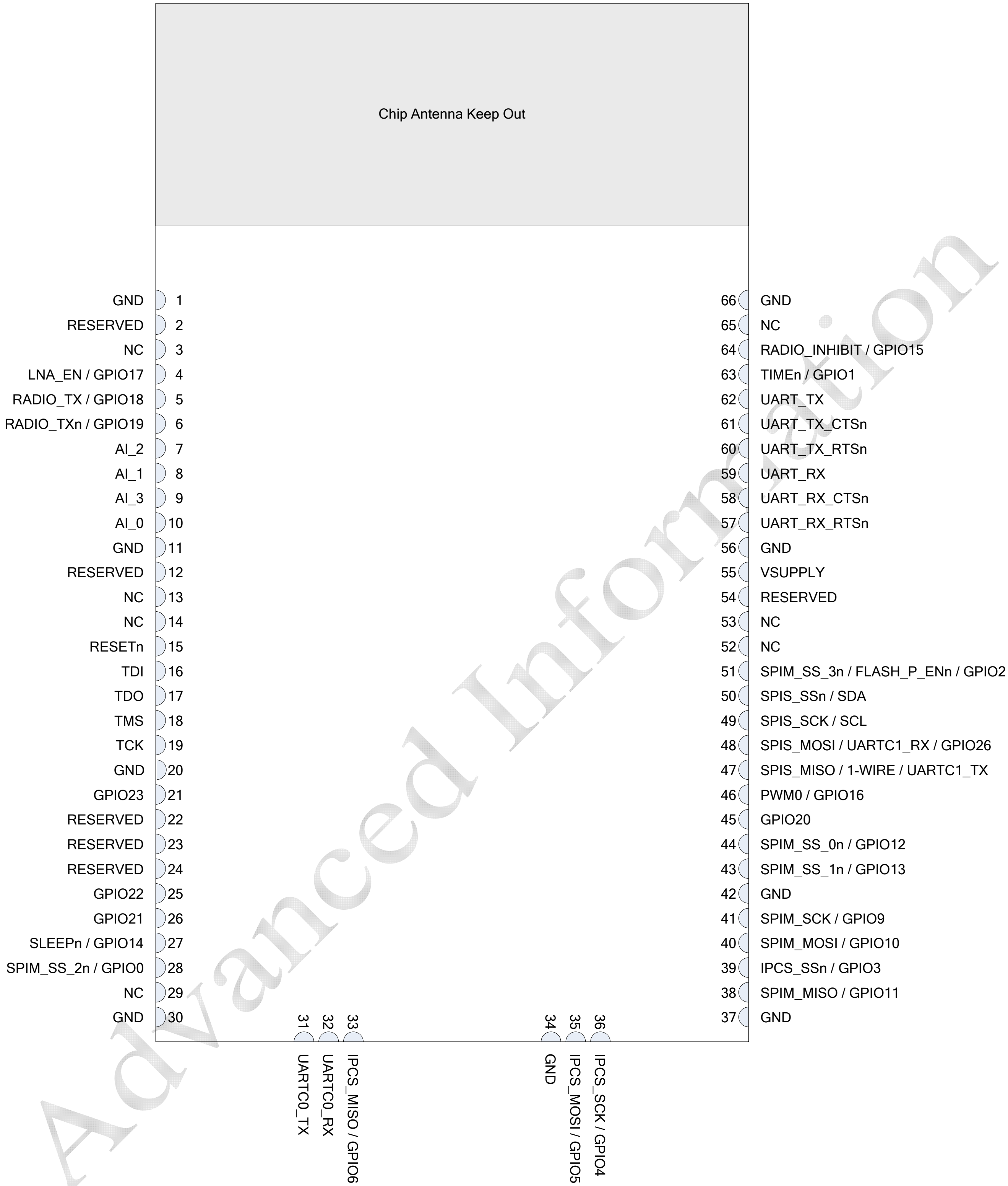


Figure 5 M6001 – Mote Module with Chip Antenna

Table 2 ***M600x* Mote Module Pinout Assignments**

No	Power Supply	Type	I / O	Description
1	GND	Power	-	Ground
11	GND	Power	-	Ground
20	GND	Power	-	Ground
30	GND	Power	-	Ground
34	GND	Power	-	Ground
37	GND	Power	-	Ground
42	GND	Power	-	Ground
56	GND	Power	-	Ground
66	GND	Power	-	Ground
55	VSUPPLY	Power	-	Power supply input to the M600x
No	**Radio**	**Type**	**I / O**	**Description**
4	LNA_EN GPIO17	1	O I/O	External LNA enable General purpose digital I/O
5	RADIO_TX GPIO18	1	O I/O	Radio TX active (external PA enable/switch control) General purpose digital I/O
6	RADIO_TXn GPIO19	1	O I/O	Radio TX active (external PA enable/switch control), active low General purpose digital I/O
64	RADIO_INHIBIT GPIO15	1	I I/O	Radio Inhibit General purpose digital I/O
No	**Analog**	**Type**	**I / O**	**Description**
10	AI_0	Analog	I	Analog input 0
8	AI_1	Analog	I	Analog input 1
9	AI_3	Analog	I	Analog input 3
7	AI_2	Analog	I	Analog input 2
No	**General**	**Type**	**I / O**	**Description**
15	RESETn	1	I	Reset, Input, active low
No	**JTAG**	**Type**	**I / O**	**Description**
16	TDI	1	I	JTAG test data in
17	TDO	1	O	JTAG test data out
18	TMS	1	I	JTAG test mode select
19	TCK	1	I	JTAG test clock
No	**GPIO**	**Type**	**I / O**	**Description**
21	GPIO23	1	I/O	General purpose digital I/O
25	GPIO22	1	I/O	General purpose digital I/O
26	GPIO21	1	I/O	General purpose digital I/O
45	GPIO20	1	I/O	General purpose digital I/O
Note: See also pins 4, 5, 6, 27, 28, 33, 35, 36, 38, 39, 40, 41, 43, 44, 46, 48, 51, 63 and 64 for additional GPIO ports.				
No	**CLI**	**Type**	**I / O**	**Description**
31	UARTC0_TX	2	O	CLI UART 0 transmit
32	UARTC0_RX	1	I	CLI UART 0 receive

No	UART	Type	I/O	Description
57	UART_RX_RTSn	1	I	UART receive (RTS) request to send, active low
58	UART_RX_CTSn	1	O	UART receive (CTS) clear to send, active low
59	UART_RX	1	I	UART receive
60	UART_TX_RTSn	1	O	UART transmit (RTS) request to send, active low
61	UART_TX_CTSn	1	I	UART transmit (CTS) clear to send, active low
62	UART_TX	2	O	UART transmit

No	SPI Master	Type	I/O	Description
28	SPIM_SS_2n GPIO0	1	O I/O	SPI master slave select 2, active low General purpose digital I/O
38	SPIM_MISO GPIO11	1	I I/O	SPI master (MISO) master in slave out port General purpose digital I/O
40	SPIM_MOSI GPIO10	2	O I/O	SPI master (MOSI) master out slave in port General purpose digital I/O
41	SPIM_SCK GPIO9	2	O I/O	SPI master (SCK) serial clock port General purpose digital I/O
43	SPIM_SS_1n GPIO13	1	O I/O	SPI master slave select 1, active low General purpose digital I/O
44	SPIM_SS_0n GPIO12	1	O I/O	SPI master slave select 0, active low General purpose digital I/O
51	SPIM_SS_3n FLASH_P_ENn GPIO2	1	O I I/O	SPI master slave select 3, active low. Flash program enable, active low Note that this functionality is available only when RESETn is asserted General purpose digital I/O
No	**SPI Slave/FLASH Programming**	**Type**	**I/O**	**Description**
33	IPCS_MISO GPIO6	2	O I/O	SPI flash emulation (MISO) master in slave out port General purpose digital I/O
35	IPCS_MOSI GPIO5	1	I I/O	SPI flash emulation (MOSI) master out slave in port General purpose digital I/O
36	IPCS_SCK GPIO4	1	I I/O	SPI flash emulation (SCK) serial clock port General purpose digital I/O
39	IPCS_SSn GPIO3	1	I I/O	SPI flash emulation slave select, active low General purpose digital I/O
Note: See also pin 55 under SPI master for FLASH_P_ENn functionality.				
No	**Special Purpose Digital**	**Type**	**I/O**	**Description**
27	SLEEPn GPIO14	1 1	I I/O	Deep Sleep, active low General purpose digital I/O
46	PWM0 GPIO16	2	O I/O	Pulse width modulator 0 General purpose digital I/O
63	TIMEn GPIO1	1	I I/O	Time capture request, active low General purpose digital I/O

No	I^2C / 1-Wire / SPI Slave 2	Type	I / O	Description
47	SPIS_MISO 1-WIRE UARTC1_TX	2	O IO O	SPI slave (MISO) master in slave out port 1-Wire UART 1 transmit
48	SPIS_MOSI UARTC1_RX GPIO26	1	I I I/O	SPI slave (MOSI) master out slave in port UART 1 receive General purpose digital I/O
49	SPIS_SCK SCL	2	I I/O	SPI slave (SCK) serial clock port I^2C serial clock
50	SPIS_SSn SDA	2	I I/O	SPI slave select, active low I^2C serial data
Note: The following pins are reserved or NC and should not be connected: 2, 3, 12, 13, 14, 22, 23, 24, 29, 52, 53, 54, and 65.				

3.3 Power Supply

The DN6000/M600x is powered from a single pin, VSUPPLY, generating all the internally required supplies. With two integrated DC/DC converters and four voltage regulators, the sensitivity to noise on VSUPPLY is minimal. However, during typical operation the DN6000/M600x will vary its load on the power supply from the µA range to 10's of mA over a few µs. During such transients, it is important that the power supply be able to meet the device's specifications for supply noise tolerance. The DN6000/M6000 is designed to operate with specific decoupling capacitance on VCORE, VDDA, VOSC, VDDPA, and VPRIME. Use of the correctly sized ceramic capacitors is important for normal operation.

3.3.1 Power-on Reset Voltage Supervision

The DN6000/M600x will enter power-on-reset state when VSUPPLY dips below 1.5 V and will remain there until this minimum voltage is applied to VSUPPLY.

3.4 Radio

The DN6000/M600x has the lowest powered commercially available 2.4 GHz 802.15.4e-compliant radio. It has an integrated power amplifier (PA) that can generate up to 8 dBm output power. External PA support is provided via the LNA_EN, RADIO_TX, and RADIO_TXn pins. External input is also provided, which acts as a digital interrupt to enable an external controller to temporarily disable the radio software driver via the RADIO_INHIBIT pin.

3.4.1 Antenna

The DN6000/M6000 allows direct connection to a single-ended 50-Ohm antenna, or optionally to an external PA/LNA circuit. It incorporates a TX/RX switch, and because the transmit and receive signals are single-ended, a balun (and its associated transformer efficiency losses) are not required. With an on-board integrated PA, the DN6000/M6000 provides options to set typical output power to 0 dBm or to +8 dBm. In addition, the DN6000/M6000 can be configured to drive optional control signals for an external PA and/or LNA. The antenna must meet the specifications in Table 3. For further details on radio transmit and receive, see section 1.1.

Table 3 Antenna Specifications

Parameter	Value
Frequency range	2.4–2.4835 GHz
Impedance	50 Ω
Maximum VSWR	3:1
Antenna jack (M6000)	U.FL
Chip antenna (M6001)	*TBD*

3.5 Analog

The DN6000/M600x has four analog inputs. Its 10-bit ADC includes a 4-bit DAC for adjusting offset and a 3-bit VGA, as shown in Figure 6. The software application layer controls ADC operation and may be configured to automatically sample any combination of the internal temperature sensor, or analog input signals.

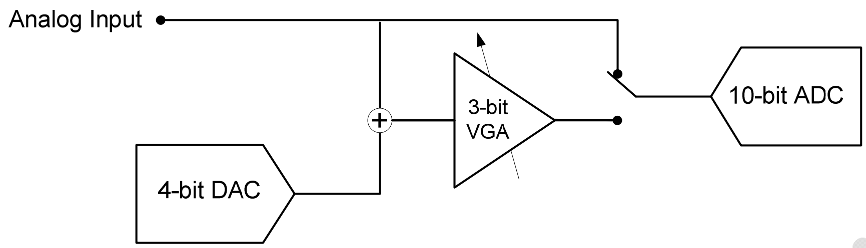


Figure 6 Analog to Digital Chain

3.6 Crystal

The DN6000/M6000 includes three clock sources: a low power oscillator designed for a 32.768 kHz crystal, the radio reference oscillator designed for a 20 MHz crystal, and an internal relaxation oscillator.

3.6.1 32.768 kHz Crystal Source

Once the DN6000/M600x is powered up and the 32.768 kHz crystal source has begun oscillating, the 32.768 kHz crystal remains operational while in the Active state, and is used as the timing basis when in Doze state.

3.6.2 20 MHz Crystal Source

The 20 MHz crystal source is used predominately when the radio is operational, and is automatically enabled and disabled by the PMU as needed. The 20 MHz source can also be used as the reference for internal ADC timing, and the Pulse Width Modulator (PWM).

3.6.3 Relaxation Oscillator

The internal relaxation oscillator is the primary clock source for the core of the DN6000/M600x, providing the clock for the ARM Cortex-M3 and the instruction and data busses between the CPU and all peripherals. The internal relaxation oscillator typically starts up in less than 5 µs, providing a low energy method for changing states from Doze to Active. This quick change allows the DN6000/M600x to wake up and receive data over the UART and SPI slave by simply by detecting activity on one of the appropriate signals. The DN6000/M600x includes an intelligent set of dividers that allow dynamic scaling of the system clock, while maintaining constant frequencies for those systems that require an accurate timing reference, such as the flash controller and UARTs.

3.7 Reset

The RESETn input pin is internally pulled up. Given the DN6000/M600x's internal power-on reset circuit, externally driving RESETn is optional. Note that for a graceful shutdown, it is recommended that the software and networking layers be cleanly halted prior to assertion of the RESETn pin.

3.8 JTAG

The DN6000/M600x includes an IEEE 1149.1-compliant JTAG port for boundary scan.

3.9 GPIOs

The DN6000/M6000 supports up to 23 General Purpose Input/Output pins. The DN6000/M6000 GPIO pins supports the following configurations:

- GPIO_PEx—Pull enable for GPIOx
- GPIO_PDx—Pull direction for GPIOx
- GPIO_OEx—Operate as open drain for GPIOx
- GPIO_STRNx—Select low or high drive strength for GPIOx
- GPIO_IEx—Enable input of for GPIOx (disabling inputs minimizes leakage on floating inputs)
- GPIO_OUT_SETx—Set GPIOx output to VSUPPLY
- GPIO_OUT_CLRx—Set GPIOx output to VSS

These pin configurations are settable via the software application layer.

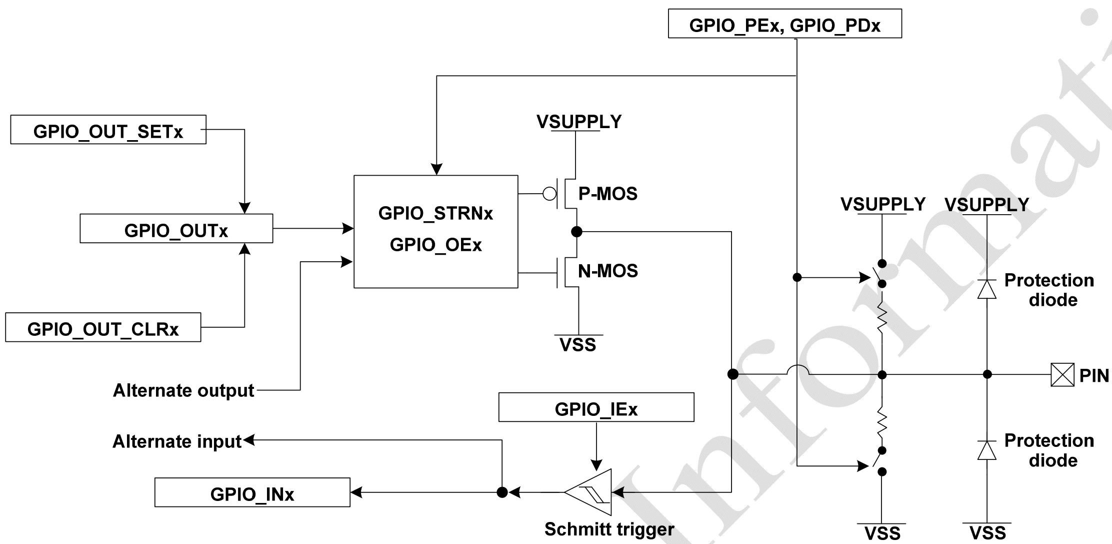


Figure 7 GPIO Configuration

In addition to the functionality shown in Figure 7, the GPIOs can be individually configured as either an active high or active low interrupt, each capable of waking the system from Doze or Deep Sleep. For additional information on system modes and duty cycling, see section 2.0.

3.10 Pulse Width Modulation

The DN6000/M600x supports a pulse width modulated output (pin PWM0). Refer to the API guide for details.

3.11 Time

The DN6000/M600x has the ability to deliver network-wide synchronized timestamps. The DN6000/M600x sends a time packet through its serial interface when one of the following occurs:

- Mote receives an HDLC request to read time
- The TIMEn signal is asserted

The use of TIMEn is optional and has the advantage of being more accurate. The value of the timestamp is captured in hardware relative to the rising edge of TIMEn. If the HDLC request is used, due to packet processing the value of the timestamp may be captured several milliseconds after receipt of the packet.

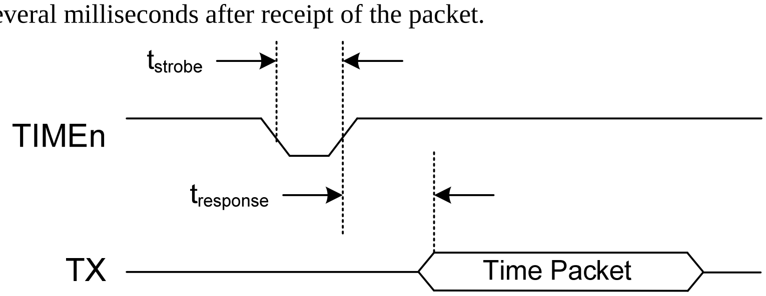


Figure 9 Timestamp Timing Diagram

Table 4 Timestamp Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at to 25 °C, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Unit
t_{strobe}		125			µs
$t_{response}$	From rising edge of TIMEn			100	ms
Network wide accuracy			5		µs

3.12 External Deep Sleep Control

The DN6000/M600x provides input signals to enable an external controller to put the DN6000/M600x into and out of Deep Deep Sleep state. When the DEEP SLEEPn pin is asserted, the DN6000/M600x will enter low power Deep Sleep state. Asserting any pin configured as a digital input interrupt will wake the DN6000/M600x from Deep Sleep state to Active. For details on operating modes, see section 2.0.

3.13 UARTs

The DN6000/M600x includes three UARTs: the API UART, UARTC0, and UARTC1, all of which are optimized to support operation consistently during both the Doze and Active states of operation.

Each UART supports the following:

- Configurable baud rate
- Even/Odd/No parity
- 1 or 2 stop bits
- 16x over-sampling with noise filtering
- Transmit scatter/gather DMA
- UARTC0 and UARTC1 support a four-byte receive FIFO and are limited to 9600 baud. In addition, the API UART supports:
- Receive scatter/gather DMA
- HDLC support in hardware
- Support of rates to 115.2 kBaud with only 2 wires when HDLC is enabled

Table 5 UART Details

UART Port	Pins	Software Function
UART (API)		API
UART (CLI)	UARTC0_TX, UARTC0_RX	CLI for debugging and troubleshooting
UART1	UARTC1_TX, UARTC1_RX	Reserved for future use

3.13.1 UART Protocols

In a system design with more than one device communicating across a serial port, higher serial data rates translate into lower power consumption. In addition to receive and transmit signals the DN6000/M600x provides an additional pair of signals, UART_TX_RTSn and UART_TX_CTSn, to support low power implementations when the DN6000/M600x is connected to another low power microcontroller. The enabling/disabling of UART_TX_RTSn and UART_TX_CTSn, is accomplished via the tx_handshake command defined in IP Mote CLI Commands Guide. When these pins are enabled, the DN6000/M600x asserts the active low UART_TX_RTSn, transmit request to send, and waits for the assertion of UART_TX_CTSn prior to transmitting the packet. For details on the timing of the UART protocol, see section 6.12 (UART AC timing).

3.14 SPI Master

The SPI master supports all combinations of shifting MSB to LSB, LSB to MSB, CPOL, and CPHA, as defined in Figure 10. In addition, the SPI master working in concert with the PWM output signal can be set up to support repetitively sampled data from one or more channels of an external ADCs with a low jitter time base. The SPI Master can support up to 4 slaves.

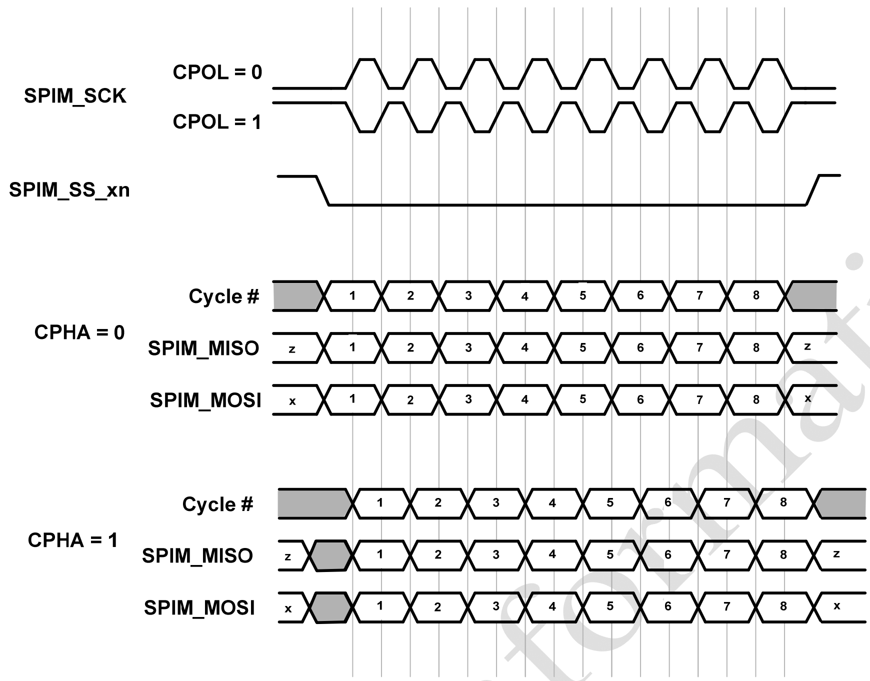


Figure 10 SPI Supported Clock Polarity and Phase Configurations, LSBFE (least significant bit first enable) = 1

3.15 1-Wire

The DN6000/M600x provides a 1-Wire module, a device communications bus system that provides low-speed data, signaling and power over a single wire. 1-Wire is similar in concept to I²C, but with lower data rates and longer range.

3.16 I^{2}C Master

The DN6000/M600x provides an Inter-Integrated Circuit (I^{2}C) module, which is a two-wire, serial data (SDA) and serial clock (SCL), bidirectional serial bus. The I^{2}C module supports the following features:

- Master mode
- Software-programmable bit clock frequency up to 369 kbps
- On-chip noise filtering

3.17 Flash Programming

To support in-circuit programming, the DN6000/M600x can present itself as a serial flash device on the IPCS_SSn, IPCS_SCK, IPCS_MOSI, and IPCS_MISO pins.

3.18 SPI Slave

The DN6000/M600x provides for an additional SPI slave port in addition to the flash programming port. Refer to the SPI Slave AC Timing in section 6.11.

3.19 Fuse Table

The DN6000/M600x family includes hardware support for configuration of the device immediately following power on reset based upon a data structure stored in the first page of flash. The fuse table allows for configuration of IO, preventing IO leakage from negatively affecting current consumption during power on, which can be a significant issue for current limited supplies. The page sized binary image for a fuse table is created separately from the code image and is either separately written or pre-pended to DN6000/M600x code image.

3.20 Temperature Sensor

The DN6000/M600x has an on-board temperature sensor. The temperature readings are available locally through the mote serial API and through the network at the manager via the manager API.

4.0 Absolute Maximum Ratings

The absolute maximum ratings shown in Table 6 should not be violated under any circumstances. Permanent damage to the device may be caused by exceeding one or more of these parameters. Unless otherwise noted, all voltages in Table 6 are made relative to VSS.

Table 6 Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units	Comments
Supply voltage (VSUPPLY to VSS)	–0.3		3.75	V	
Voltage on any digital I/O pin	–0.3		VSUPPLY + 0.3 up to 3.75	V	
Input RF level			10	dBm	Input power at antenna connector
Storage temperature range	–40		+125	°C	Extended storage above 105 deg C will reduce the device's operating life
Lead temperature			+245	°C	For 10 seconds
VSWR of antenna			3:1		
ESD protection					
Antenna pad			±700	V	HBM
All other pads			±2000	V	HBM
			±200	V	CDM

Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

5.0 Recommended Operating Conditions

Table 7 Recommended Operating Conditions

Parameter	Min	Typ	Max	Units	Comments
Operational supply voltage range (between VSUPPLY and VSS)	2.1	3.6	3.75	V	Including noise and load regulation
Voltage supply noise			250	mV_{p-p}	50 Hz to 2 MHz
Operating temperature range	–40		+85	°C	
Operating relative humidity	10		90	% RH	Non-condensing
Power on Reset threshold		1.5		V	
Temperature ramp	-8		+8	°C/min	

6.0 Electrical Characteristics

6.1 Detailed Radio Specifications

The following characteristics are measured with VSUPPLY = 3.6 V at to 25 °C, unless otherwise specified.

Table 8 Detailed Radio Specifications

Parameter	Conditions	Min	Typ	Max	Units
Operating frequency	As specified by [1]	2.4000		2.4835	GHz
Number of channels			15		
Channel separation	As specified by [1]		5		MHz
Occupied channel bandwidth	At –20 dBc		2.7		MHz
Modulation	IEEE 802.15.4 DSSS				
Raw data rate	As specified by [1]		250		kbps
Range* Indoor† Outdoor† Free space	25 °C, 50% RH, +2 dBi omni-directional antenna		 100 300 1200		 m m m
* Actual RF range performance is subject to a number of installation-specific variables including, but not restricted to ambient temperature, relative humidity, presence of active interference sources, line-of-sight obstacles, near-presence of objects (for example, trees, walls, signage, and so on) that may induce multipath fading. As a result, actual performance varies for each instance. † 1 meter above ground.					

6.2 DC Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at to 25 °C, unless otherwise specified.

Table 9 DN6000/M6000 Current Consumption

Parameter	Conditions	Min	Typ	Max	Units
Reset	After power-on reset		1.2		µA
Deep Sleep			0.8		µA
Doze	RAM on; ARM Cortex-M3, flash, radio, and peripherals off, all data and state retained, 32.768 kHz reference active		1.2		µA
Serial Flash Emulation			20		mA
Peak Operating current at 8 dBm output power at 0 dBm output power	System operating at 14.7 MHz Radio Tx Flash Write			 30 26	 mA mA
Active*	ARM Cortex-M3, RAM, and flash on; radio and peripherals off CLK = 7.37 MHz, Vcore = 1.8 V		2.4		mA
Flash write	Single bank write		3		mA
Flash erase	Single bank page or mass erase		2.5		mA

Parameter	Conditions	Min	Typ	Max	Units
Radio Tx†	Mesh Network - CLK = 7.3728 MHz, AES active 0 dBm output power 8 dBm output power		 5.4 9.7		 mA mA
Radio Rx†	Mesh Network - CLK = 7.3728 MHz, AES active		4.5		mA
Note: See section 2.0 for detailed definitions of modes. * CLK = Clock frequency of CPU and peripherals. † CPU idle.					

6.3 Radio Receive Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at to 25 °C, unless otherwise specified.

Table 10 Radio Receive Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Frequency range		2.4000		2.4835	GHz
Receiver sensitivity	PER = 1%, as specified by [1]		–91		dBm
Saturation (maximum input level)			0		dBm
Adjacent channel rejection (high side)	Desired signal at -82 dBm, adjacent modulated channel at 5 MHz, PER = 1%, as specified by [1]		22		dBc
Adjacent channel rejection (low side)	Desired signal at -82 dBm, adjacent modulated channel at -5 MHz, PER = 1%, as specified by [1]		19		dBc
Alternate channel rejection (high side)	Desired signal at -82 dBm, adjacent modulated channel at 10 MHz, PER = 1%, as specified by [1]		40		dBc
Second alternate channel rejection (high side)	Desired signal at -82 dBm, adjacent modulated channel at 10 MHz, PER = 1%, as specified by [1]		42		dBc
Alternate channel rejection (low side)	Desired signal at -82 dBm, adjacent modulated channel at -10 MHz, PER = 1%, as specified by [1]		36		dBc
Second alternate channel rejection (low side)	Desired signal at -82 dBm, adjacent modulated channel at 10 MHz, PER = 1%, as specified by [1]		42		dBc
Co-channel rejection	Desired signal at -82 dBm. Undesired signal is 802.15.4 modulated at same frequency. PER = 1%.		–6		dBc
LO feed through			<–47		dBm
Frequency error tolerance	[1] requires ±40		±50		ppm
Symbol rate error tolerance			±50		ppm
RSSI input range			–10 to –90		dBm
RSSI accuracy			±4		dB
RSSI resolution			1		dB

6.4 Radio Transmitter Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at to 25 °C, unless otherwise specified.

Table 11 Radio Transmitter Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Output power Calibrated settings	Delivered to a 50 Ω load, over temperature and voltage ranges		0 8		dBm dBm
Frequency range*		2.4000		2.4835	GHz
Spurious emissions 30 MHz to 1000 MHz 1 GHz to 12.75 GHz	Conducted measurement with a 50 Ω single-ended load, +8 dBm output power		<–47 <–35		dBm dBm
2nd Harmonic	Delivered to a 50 Ω load		–35		dBm
3rd Harmonic	Delivered to a 50 Ω load		–38		dBm

* Actual RF range performance is subject to a number of installation-specific variables including, but not restricted to ambient temperature, relative humidity, presence of active interference sources, line-of-sight obstacles, near-presence of objects (for example, trees, walls, signage, and so on) that may induce multipath fading. As a result, actual performance varies for each instance.

6.5 Digital I/O Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at to 25 °C, unless otherwise specified.

Table 12 Digital I/O Type 1

Parameter	Conditions	Min	Typ	Max	Units
V_{IL} (low-level input voltage)		–0.3		0.6	V
V_{IH} (high-level input voltage)		VSUPPLY - 0.3		VSUPPLY + 0.3	V
V_{OL} (low-level output voltage)	$I_{OL(max)}$ = 1.2 mA			0.4	V
V_{OH} (high-level output voltage)	$I_{OH(max)}$ = −1.8 mA	VSUPPLY - 0.3		VSUPPLY + 0.3	V
Input leakage current			50		nA

Table 13 Digital I/O Type 2

Parameter	Conditions	Min	Typ	Max	Units
V_{IL} (low-level input voltage)		–0.3		0.6	V
V_{IH} (high-level input voltage)		VSUPPLY - 0.3		VSUPPLY + 0.3	V
V_{OL} (low-level output voltage) Low Drive	$I_{OL(max)}$ = 2.2 mA			0.4	V
V_{OH} (high-level output voltage) Low Drive	$I_{OH(max)}$ = −3.2 mA	VSUPPLY - 0.3		VSUPPLY + 0.3	V
V_{OL} (low-level output voltage) High Drive	$I_{O(max)}$ = 4.5 mA			0.4	V
V_{OH} (high-level output voltage) High Drive	$I_{OH(max)}$ = −6.3 mA	VSUPPLY - 0.3		VSUPPLY + 0.3	V
Input leakage current			50		nA

6.6 Temperature Sensor Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at to 25 °C, unless otherwise specified.

Table 14 Temperature Sensor Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Offset	Temperature offset error at 25 ºC		±0.25		°C
Slope error	Slope error from -40 to +85 ºC		±0.033		°C/°C
Current consumption			65		µA

6.7 ADC Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at to 25 °C, unless otherwise specified.

Table 15 ADC Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Variable gain amplifier					
Gain		1		8	
Gain error				1	%
Digital to analog converter (DAC)					
Offset output		1.8/16		1.8	V
Differential non-linearity (DNL)				7.2	mV
Analog to digital converter (ADC)					
Full-scale, signal			1.80		V
Resolution			1.8		mV
Offset	Midscale			±4	LSB
Differential non-linearity (DNL)				1	LSB
Integral non-linearity (INL)				1	LSB
Settling time	10-kOhm source impedance			10	µs
Conversion time				20	µs
Current consumption				50	µA
Analog Inputs*					
Load			17	35	pF
Input resistance			1	2	kOhm

* The analog inputs to the ADC can be model as a series resistor to a load capacitor. At a minimum the entire circuit, including the source impedance for the signal driving the analog input should be designed to settle to within ¼ LSB within the sampling window to match the performance of the ADC.

6.8 System Characteristics

The following characteristics are measured with VSUPPLY = 3.6 V at to 25 °C, unless otherwise specified.

Table 16 System Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Doze to Active state delay			5		µs
Doze to Radio TX or RX			1.2		ms
Radio RX to TX and TX to RX turnaround				192	µs
Q_{CCA} charge to sample RF channel	Start from Doze state		4		µC
Radio baud rate			250	2000	kbps
RESETn pulse width		125			µs

6.9 FLASH AC Timing

The following characteristics are measured with VSUPPLY = 3.6 V at to 25 °C, unless otherwise specified.

Table 17 FLASH AC Timing Values

Parameter	Conditions	Min	Typ	Max	Unit
$t_{32\text{-}BIT\_WORD}$	Writing a 32-bit word			21	µs
t_{PAGE_ERASE}	Page Erase			21	ms
t_{MASS_ERASE}	Bank Erase			21	ms

6.10 SPI Master AC Timing

The following characteristics are measured with VSUPPLY = 3.6 V at to 25 °C, unless otherwise specified.

Table 18 SPI Master AC Timing Values

Parameter	Conditions	Min	Typ	Max	Unit
t_{SSS}	SPIM_SSn setup to leading edge of SPIM_SCK	115			ns
t_{SSH}	SPIM_SSn hold from trailing edge of SPIM_SCK	115			ns
t_{CK}	SPIM_SCK period	115			ns
t_{DIS}	SPIM_MISO data setup	15			ns
t_{DIH}	SPIM_MISO data hold	5			ns
t_{DOV}	SPIM_MOSI data valid	-5		15	ns

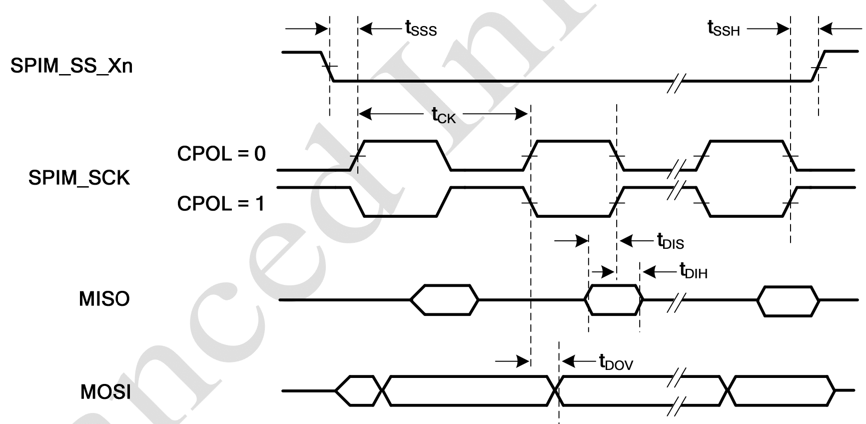


Figure 11 SPI Master Timing – CPHA = 0

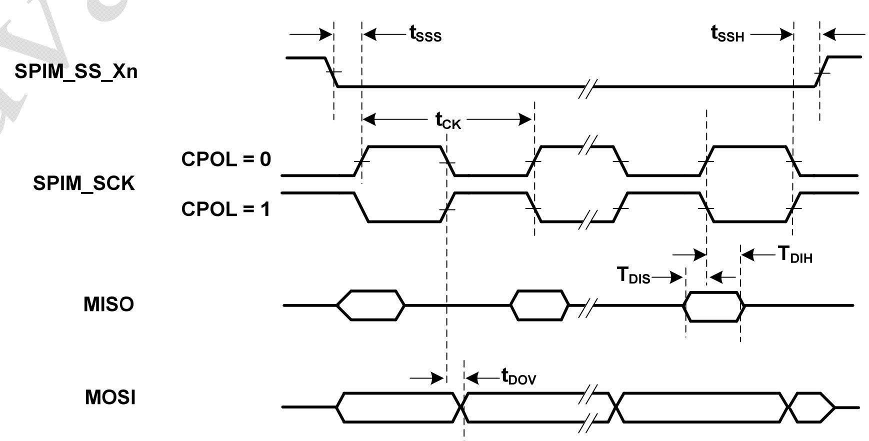


Figure 12 SPI Master Timing – CPHA = 1

6.11 SPI Slave AC Timing

The following characteristics are measured with VSUPPLY = 3.6 V at to 25 °C, unless otherwise specified.

Table 19 SPI Slave AC Timing Values

Parameter	Conditions	Min	Typ	Max	Unit
t_{SSS}	SPIS_SSn setup to leading edge of SPIS_SCK	15			ns
t_{SSH}	SPIS_SSn hold from trailing edge of SPIS_SCK	15			ns
t_{CK}	SPIS_SCK period Active state Doze state	 125 5000			 ns ns
t_{DIS}	SPIS_MOSI data setup	15			ns
t_{DIH}	SPIS_MOSI data hold	5			ns
t_{DOV}	SPIS_MISO data valid	0		15	ns
t_{OFF}	SPIS_MISO data tri-state	0		15	ns

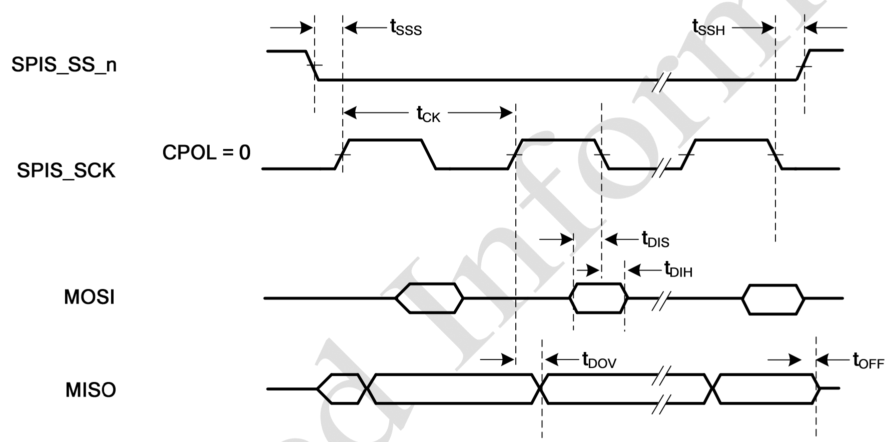


Figure 13 SPI Slave Timing – CPHA = 0

6.12 UART AC Timing

The following characteristics are measured with VSUPPLY = 3.6 V at to 25 °C, unless otherwise specified.

Table 20 UART Timing Values

Parameter	Conditions	Min	Typ	Max	Unit
t_{RX_BAUD}	Deviation from baud rate	–2		+2	%
t_{TX_BAUD}	Deviation from baud rate	–1		+1	%
$t_{RX\_RTS\_R \text{ to } RX\_CTS}$	Assertion of UART_RX_RTSn to assertion of UART_RX_CTSn, or negation of UART_RX_RTSn to negation of UART_RX_CTSn	0		22	ms
$t_{CTS\_R \text{ to } RX}$	Assertion of UART_RX_CTSn to start of byte	0		20	ms
$t_{EOP \text{ to } RX\_RTS}$	End of packet (end of the last stop bit) to negation of UART_RX_RTSn	0		22	ms
$t_{TX\_RTS\_T \text{ to } TX\_CTS}$	Assertion of UART_TX_RTSn to assertion of UART_TX_CTSn, or negation of UART_TX_RTSn to negation of UART_TX_CTSn	0		22	ms
$t_{TX\_CTS\_T \text{ to } TX}$	Assertion of UART_TX_CTSn to start of byte	0		2	bit period

Parameter	Conditions	Min	Typ	Max	Unit
$t_{EOP\ to\ TX\_RTS}$	End of packet (end of the last stop bit) to negation of UART_TX_RTSn	0		1	bit period
$t_{RX\_INTERBYTE}$	Interbyte delay			100	ms
$t_{TX\ to\ TX\_CTS}$	Start of byte to negation of UART_TX_CTSn	0			ms

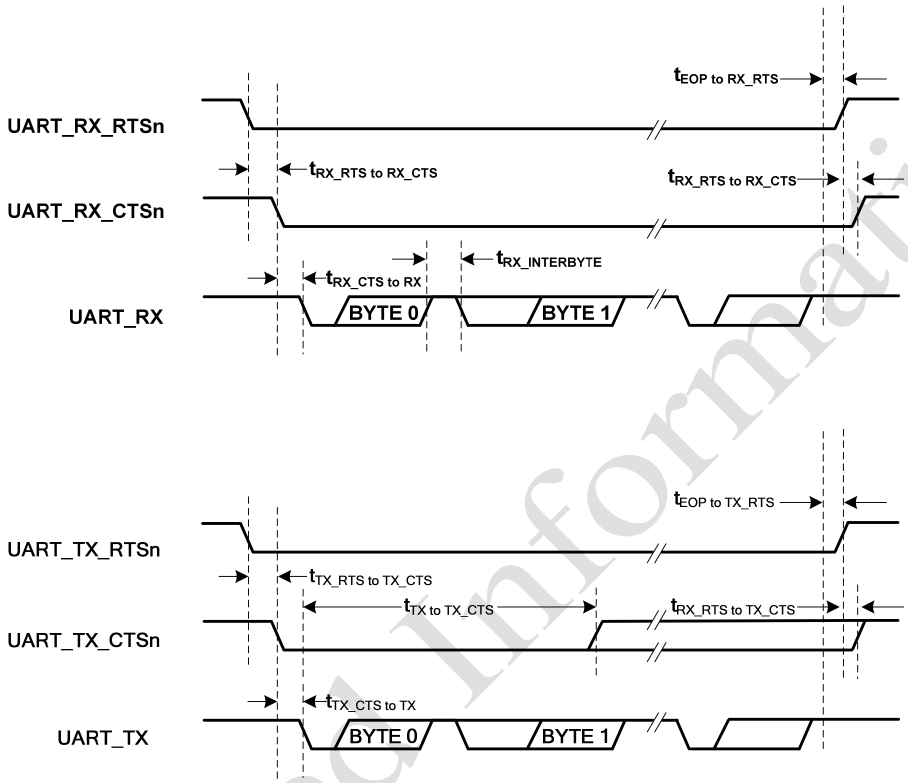


Figure 14 UART Timing

6.13 I²C AC Timing

The following characteristics are measured with VSUPPLY = 3.6 V at to 25 °C, unless otherwise specified.

Table 21 I²C AC Timing Values

Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}				369	kHz
t_{HD_STA}	$f_{SCL} \leq 100$ kHz $f_{SCL} > 100$ kHz	4.0 0.6			µs µs
t_{SU_STA}	$f_{SCL} \leq 100$ kHz $f_{SCL} > 100$ kHz	4.7 0.6			µs µs
t_{HD_DAT}		0			ns
t_{SU_DAT}		250			ns
t_{SU_STO}		4.0			µs

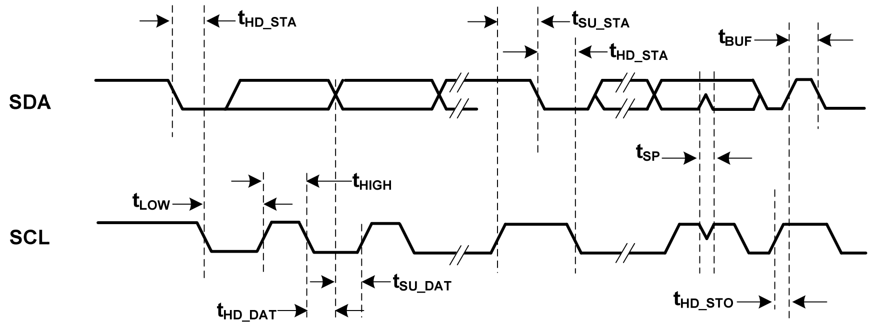
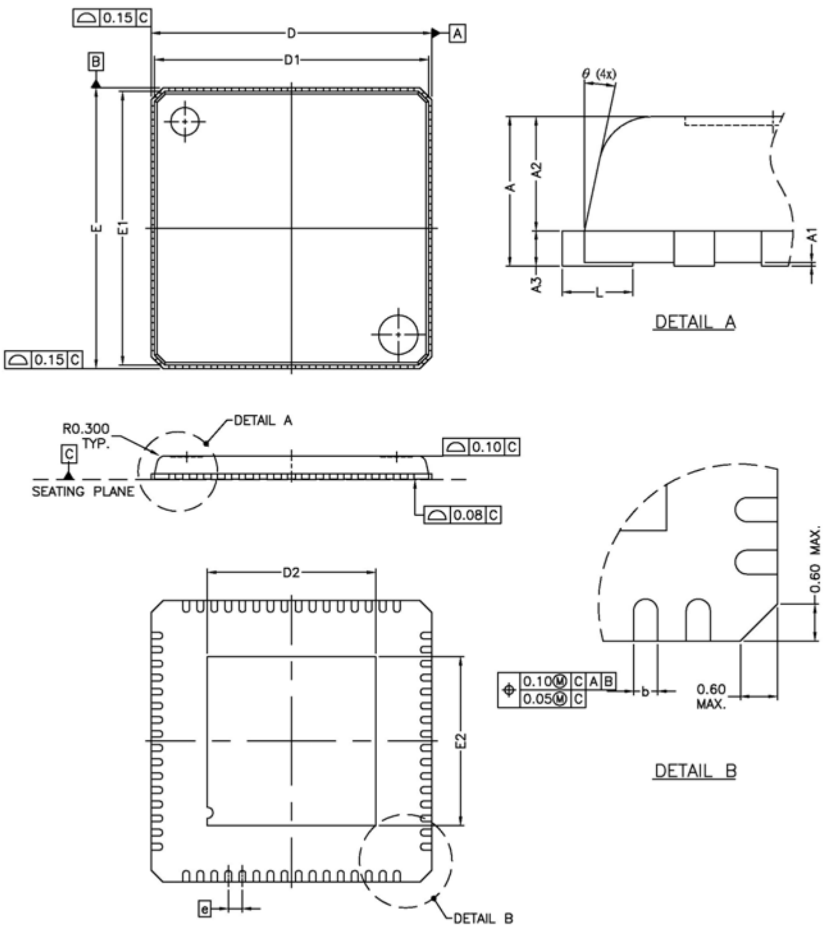


Figure 15 I²C Timing

7.0 Mechanical Details

7.1 Mote-on-Chip

The DN6000 comes in 72-lead 10 x 10 mm, 0.5 mm lead pitch QFN, as illustrated in Figure 16.



SYMBOL	DIMENSION (MM) MIN.	NOM.	MAX.	DIMENSION (MIL) MIN.	NOM.	MAX.
A	0.80	0.85	1.00	31	33	39
A1	0.00	0.02	0.05	0	1	2
A2	–	–	–	–	–	–
A3	–	0.20	–	–	8	–
b	0.18	0.23	0.28	7	9	11
D	10.00 BSC			394 BSC		
D1	9.75 BSC			384 BSC		
D2	5.85	6.00	6.15	230	236	242
E	10.00 BSC			394 BSC		
E1	9.75 BSC			384 BSC		
E2	5.85	6.00	6.15	230	236	242
e	0.50 BSC			20 BSC		
L	0.35	0.40	0.45	14	16	18
θ	0°	–	14°	0°	–	14°

NOTE :

1. REFER TO JEDEC STD: MO-220.
2. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

Figure 16 Mechanical Drawing – DN6000 Mote with U.FL Antenna Connector

7.2 Mote Module

The M6000 comes in 66-lead 24 x 37.465 mm, 1 mm lead pitch castellated PCB, as illustrated in Figure 17.

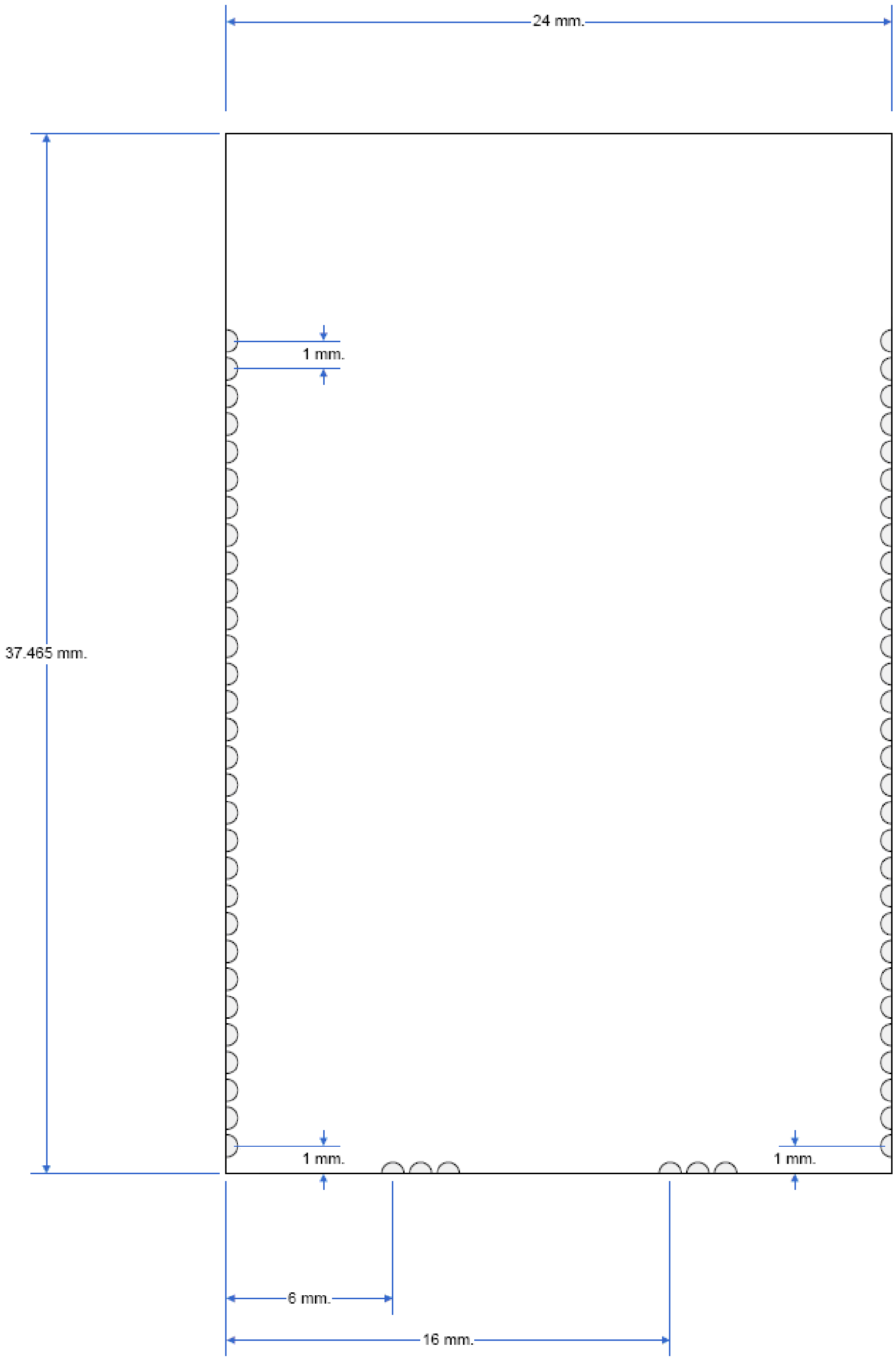


Figure 17 Mechanical Drawing – M6000 Mote with U.FL Antenna Connector

The M6001 comes in 66-lead 24 x 42 mm, 1 mm lead pitch castellated PCB, as illustrated in Figure 18.

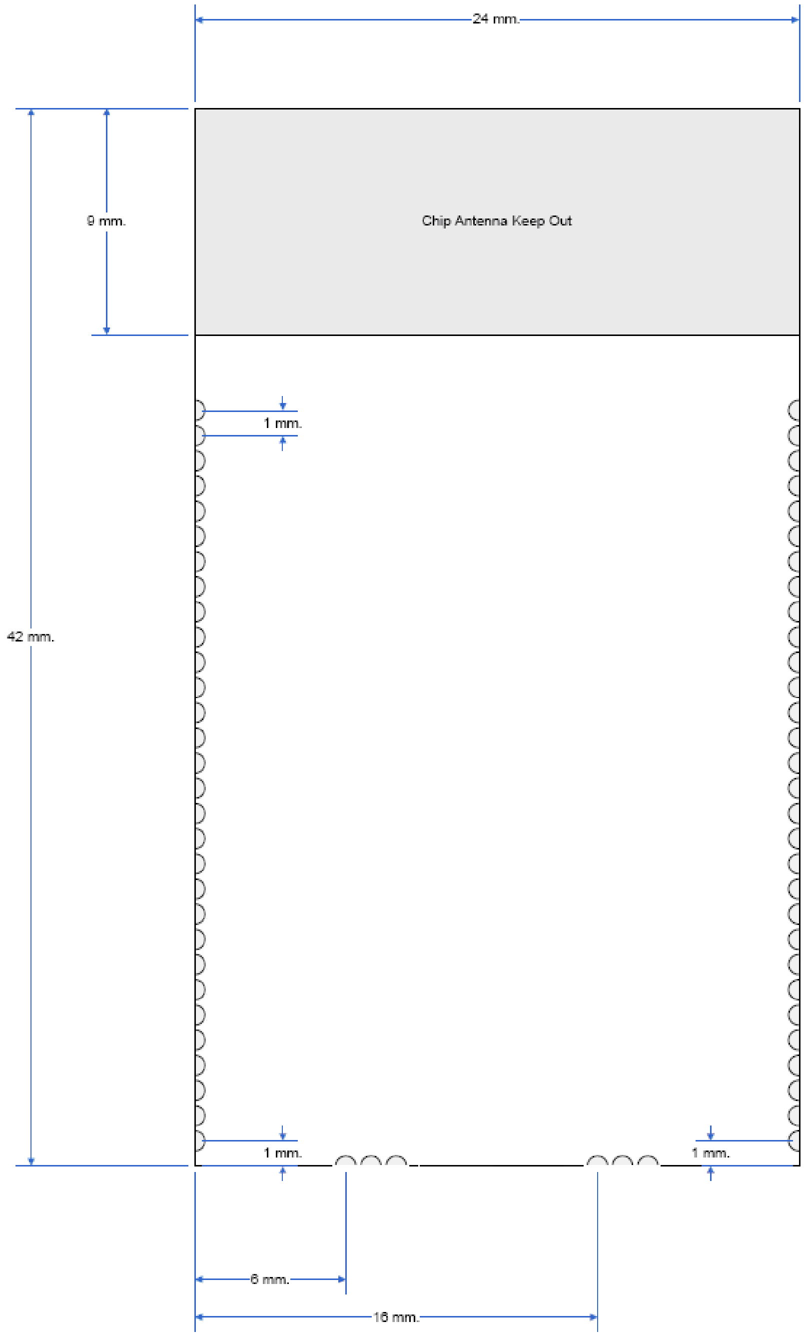


Figure 18 Mechanical Drawing – M6001 Mote with Chip Antenna Keepout

7.3 Soldering Information

The DN6000/M600x is suitable for both eutectic PbSn and RoHS-6 reflow. The maximum reflow soldering temperature is 260 ºC.

8.0 Regulatory and Standards Compliance

The DN6000/M600x is suitable for systems targeting compliance with worldwide radio frequency regulations: ETSI EN 300 328 and EN300 440 class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

8.1 Compliance to Restriction of Hazardous Substances (RoHS)

Restriction of Hazardous Substances (RoHS) is a directive that places maximum concentration limits on the use of cadmium (Cd), lead (Pb), hexavalent chromium (Cr+6), mercury (Hg), Polybrominated Biphenyl (PBB), and Polybrominated Diphenyl Ethers (PBDE). Dust Networks is committed to meeting the requirements of the European Community directive 2002/95/EC.

This product has been specifically designed to utilize RoHS-compliant materials and to eliminate or reduce the use of restricted materials to comply with 2002/95/EC.

The Dust Networks RoHS-compliant design features include:

- RoHS-compliant solder for solder joints
- RoHS-compliant base metal alloys
- RoHS-compliant precious metal plating
- RoHS-compliant cable assemblies and connector choices
- Lead-free QFN package
- Halogen-free mold compound
- RoHS-compliant and 245 °C re-flow compatible

Note: Dust Network customers may elect to use certain types of lead-free solder alloys in accordance with the European Community directive 2002/95/EC. Depending on the type of solder paste chosen, a corresponding process change to optimize reflow temperatures may be required.

9.0 References

[1] IEEE Std. 802.15.4-2006: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs) http://standards.ieee.org/getieee802/download/802.15.4-2006.pdf

10.0 Related Documentation

- *040-0102 Eterna Integration Guide*

11.0 Ordering Information

Order number for DN6000: DN6000-01EQ-Sxxx

Order number for M6000: M6000-01EP-Sxxx

Order number for M6001: M6001-01EP-Sxxx

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Document Status	Product Status	Definition
Advanced Information	Planned or under development	This datasheet contains the design specifications for product development. Dust Networks reserves the right to change specifications in any manner without notice.
Preliminary	Engineering samples and pre-production prototypes	This datasheet contains preliminary data; supplementary data will be published at a later time. Dust Networks reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. The product is not fully qualified at this point.
No Identification Noted	Full production	This datasheet contains the final specifications. Dust Networks reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not in production	This datasheet contains specifications for a product that has been discontinued by Dust Networks. The datasheet is printed for reference information only.